

CLAIMS

- 1 1. A method of forming a MOSFET device comprising:
 - 2 providing a substrate;
 - 3 forming on said substrate a relaxed SiGe layer having a Ge content between 0.51
 - 4 and 0.80; and
 - 5 depositing on said relaxed SiGe layer a ϵ -Si layer.
- 1 2. The method of claim 1, wherein said ϵ -Si layer is sized approximately at 45 Å.
- 1 3. The method of claim 1 further comprising planarizing said SiGe layer.
- 1 4. The method of claim 3, wherein said planarizing comprises CMP.
- 1 5. The method of claim 1, wherein said MOSFET device comprises a hole mobility enhancement that increases with effective vertical field.
- 1 6. The method of claim 5, wherein said hole mobility enhancement saturates approximately around 2.5.
- 1 7. The method of claim 1, wherein said ϵ -Si layer shifts the hole wave function away from the surface of said ϵ -Si layer.
- 1 8. The method of claim 1, wherein said substrate comprises a crystalline Si substrate.
- 1 9. The method of claim 1, wherein said substrate comprises a crystalline Si substrate and a relaxed SiGe graded layer.

1 10. The method of claim 1, wherein said substrate comprises a crystalline substrate and
2 an insulating layer.

1 11. The method of claim 10, wherein said insulator layer comprises an oxide.

1 12. The method of claim 1, wherein said MOSFET device comprises a PMOS device.

1 13. The method of claim 12, wherein said MOSFET device comprises a NMOS device.

1 14. The method of claim 13, wherein said PMOS and NMOS devices form a CMOS device.

1 15. The method of claim 1, wherein said relaxed SiGe layer comprises a selective
2 portion having a Ge content between 0.7 and 0.75.

1 16. A method of forming a MOSFET device comprising:

2 providing a substrate;

3 forming on said substrate a relaxed SiGe layer having a Ge content between 0.51
4 and 0.80; and

5 forming on said relaxed SiGe layer a digital alloy structure that comprises
6 alternating layers of ε-Si and SiGe having a Ge content between 0.51 and 1, wherein said
7 mobility enhancement of said device is constant.

1 17. The method of claim 16, wherein said alternating layers of SiGe and ε-Si are sized
2 approximately at 10Å.

1 18. The method of claim 16 further comprising planarizing said relaxed SiGe layer.

1 19. The method of claim 18, wherein said planarizing comprises CMP.

1 20. The method of claim 16, wherein said ϵ -Si layer shifts the hole wave function away
2 from the surface of said ϵ -Si layer.

1 21. The method of claim 16, wherein said substrate comprises a crystalline Si substrate.

1 22. The method of claim 16, wherein said substrate comprises a crystalline Si substrate
2 and a relaxed SiGe graded layer.

1 23. The method of claim 16, wherein said substrate comprises a crystalline substrate and
2 an insulating layer.

1 24. The method of claim 23, wherein said insulator layer comprises an oxide.

1 25. The method of claim 16, wherein said MOSFET device comprises a PMOS device.

1 26. The method of claim 25, wherein said MOSFET device comprises a NMOS device.

1 27. The method of claim 26, wherein said PMOS and NMOS devices form a CMOS device.

1 28. The method of claim 16, wherein said relaxed SiGe layer comprises a selective
2 portion having a Ge content between 0.7 and 0.75.

1 29. A method of forming a MOSFET device comprising:

2 providing a substrate;

3 forming on said substrate a relaxed SiGe layer having a Ge content between 0.51
4 and 0.80; and

5 depositing on said relaxed SiGe layer a ϵ -Si layer so that hole mobility
6 enhancement increases with effective vertical field.

- 1 30. The method of claim 29, wherein said ϵ -Si layer is sized approximately at 45Å.
- 1 31. The method of claim 29 further comprising planarizing said relaxed SiGe layer.
- 1 32. The method of claim 31, wherein said planarizing comprises CMP.
- 1 33. The method of claim 29, wherein said MOSFET device comprises a hole mobility
2 enhancement that increases with effective vertical field.
- 1 34. The method of claim 29, wherein said hole mobility enhancement saturates
2 approximately around 2.5.
- 1 35. The method of claim 29, wherein said ϵ -Si layer shifts the hole wave function away
2 from the surface of said ϵ -Si layer.
- 1 36. The method of claim 29, wherein said substrate comprises a crystalline Si substrate.
- 1 37. The method of claim 29, wherein said substrate comprises a crystalline Si substrate
2 and a relaxed SiGe graded layer.
- 1 38. The method of claim 29, wherein said substrate comprises a crystalline substrate and
2 an insulating layer.
- 1 39. The method of claim 38, wherein said insulator layer comprises an oxide.
- 1 40. The method of claim 29, wherein said MOSFET device comprises a PMOS device.
- 1 41. The method of claim 40, wherein said MOSFET device comprises a NMOS device.
- 1 42. The method of claim 41, wherein said PMOS and NMOS devices form a CMOS device.

- 1 43. A MOSFET device comprising:
 - 2 a substrate;
 - 3 a relaxed SiGe layer that is formed on said substrate having a Ge content between
 - 4 0.51 and 0.80; and
 - 5 a ϵ -Si layer that is deposited on said relaxed SiGe layer.
- 1 44. The MOSFET device of claim 43, wherein said ϵ -Si layer is sized approximately at
- 2 45 Å.
- 1 45. The MOSFET device of claim 43, wherein said relaxed SiGe layer is planarized.
- 1 46. The MOSFET device of claim 43 further comprising a hole mobility enhancement
- 2 that increases with effective vertical field.
- 1 47. The MOSFET device of claim 46, wherein said hole mobility enhancement saturates
- 2 approximately around 2.5.
- 1 48. The MOSFET device of claim 43, wherein said ϵ -Si layer shifts the hole wave
- 2 function away from the surface of said ϵ -Si layer.
- 1 49. The MOSFET device of claim 43, wherein said substrate comprises a crystalline Si
- 2 substrate.
- 1 50. The MOSFET device of claim 43, wherein said substrate comprises a crystalline Si
- 2 substrate and a relaxed SiGe graded layer.
- 1 51. The MOSFET device of claim 43, wherein said substrate comprises a crystalline
- 2 substrate and an insulating layer.

1 52. The MOSFET device of claim 51, wherein said insulator layer comprises an oxide.

1 53. The MOSFET device of claim 43 further comprising a PMOS device.

1 54. The MOSFET device of claim 53 further comprising a NMOS device.

1 55. The MOSFET device of claim 54, wherein said PMOS and NMOS devices form a
2 CMOS device.

1 56. The MOSFET device of claim 43, wherein said relaxed SiGe layer comprises a
2 selective portion having a Ge content between 0.7 and 0.75.

1 57. A MOSFET device comprising:

2 a substrate;

3 a relaxed SiGe layer that is formed on said substrate having a Ge content between
4 0.51 and 0.80; and

5 a digital alloy structure that is formed on said relaxed SiGe layer comprising
6 alternating layers of ε-Si and SiGe having a Ge content between 0.51 and 1, wherein said
7 mobility enhancement of said device is constant.

1 58. The MOSFET device of claim 57, wherein said alternating layers of SiGe and ε-Si is
2 sized approximately at 45Å.

1 59. The MOSFET device of claim 57, wherein said relaxed SiGe layer is planarized.

1 60. The MOSFET device of claim 57, wherein said ε-Si layer shifts the hole wave
2 function away from the surface of said ε-Si layer.

1 61. The MOSFET device of claim 57, wherein said substrate comprises a crystalline Si
2 substrate.

1 62. The MOSFET device of claim 57, wherein said substrate comprises a crystalline Si
2 substrate and a relaxed SiGe graded layer.

1 63. The MOSFET device of claim 57, wherein said substrate comprises a crystalline
2 substrate and an insulating layer.

1 64. The MOSFET device of claim 63, wherein said insulator layer comprises an oxide.

1 65. The MOSFET device of claim 57 further comprising a PMOS device.

1 66. The MOSFET device claim 65 further comprising a NMOS device.

1 67. The MOSFET device claim 66, wherein said PMOS and NMOS devices form a
2 CMOS device.

1 68. The MOSFET device of claim 57, wherein said relaxed SiGe layer comprises a
2 selective portion having a Ge content between 0.7 and 0.75.

1 69. A MOSFET device comprising:

2 a substrate;

3 a relaxed SiGe layer that is formed on said substrate having a Ge content between
4 0.51 and 0.80; and

5 a ϵ -Si layer that is deposited on said relaxed SiGe layer so that hole mobility
6 enhancement increases with effective vertical field.

1 70. The MOSFET device of claim 69, wherein said ϵ -Si layer is sized approximately at
2 45 \AA .

1 71. The MOSFET device of claim 69, wherein said relaxed SiGe layer is planarized.

1 72. The MOSFET device of claim 69, wherein said MOSFET device comprises a hole
2 mobility enhancement that increases with effective vertical field.

1 73. The MOSFET device of claim 72, wherein said hole mobility enhancement saturates
2 approximately around 2.5.

1 74. The MOSFET device of claim 69, wherein said ϵ -Si layer shifts the hole wave
2 function away from the surface of said ϵ -Si layer.

1 75. The MOSFET device of claim 69, wherein said substrate comprises a crystalline Si
2 substrate.

1 76. The MOSFET device of claim 69, wherein said substrate comprises a crystalline Si
2 substrate and a relaxed SiGe graded layer.

1 77. The MOSFET device of claim 69, wherein said substrate comprises a crystalline
2 substrate and an insulating layer.

1 78. The MOSFET device of claim 77, wherein said insulator layer comprises an oxide.

1 79. The MOSFET device of claim 69 further comprising a PMOS device.

1 80. The MOSFET device of claim 79 further comprising a NMOS device.

1 81. The MOSFET device claim 80, wherein said PMOS and NMOS devices form a
2 CMOS device.